Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of claims:

Claims 1-22. (Cancelled).

22. (Currently Amended) A method of testing an embedded electronic systems having a target processor adapted to execute a target program, the target processor being coupled to target hardware that ~~may be partially physical and partially simulated,~~ has a physical portion and a simulated portion, the method comprising:

monitoring signals present on a plurality of externally accessible terminals of the target processor as the target processor executes the target program;

determining when the target processor is attempting to access the simulated portion of the target hardware ~~on the basis of the monitored signals~~ by inputting monitored address signals into a mapping memory and outputting a stored map result from a corresponding address in the mapping memory, for each of the monitored address signals, from the mapping memory;

in response to determining that the target processor is attempting to access the simulated portion of the target hardware, suspending execution of the target program; and

in response to determining that the target processor is attempting to access the simulated portion of the target hardware, processing output signals present on a plurality of the externally accessible terminals in a hardware simulator.

23. (Currently Amended) The method of claim 22 further comprising:

determining when the target processor is attempting to access the physical portion of the target hardware ~~on the basis of the monitored signals~~ by inputting monitored address signals into a mapping memory and outputting a stored map result from a corresponding address in the mapping memory, for each of the monitored address signals, from the mapping memory; and

in response to determining that the target processor is attempting to access the physical portion of the target hardware, allowing the target processor to access the physical portion of the target hardware.

24. (Original) The method of claim 22 further comprising:

receiving input data from the hardware simulator responsive to processing the output signals;

converting the input data to corresponding input signals; and

applying the input signals to the externally accessible terminals.

25. (Cancelled).

26. (Original) The method of claim 22 wherein the step of determining when the target processor is attempting to access the simulated portion of the target hardware comprises:

monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware in the event of an access to the physical hardware by the target processor;

initiating a timing period responsive to a target hardware access by the target processor; and

detecting if the control signal is received from the physical target hardware within a predetermined period after initiating the timing period.

27. (Original) The method of claim 22 further comprising:

detecting an interrupt signal applied to the target processor during the time that the target processor has suspended execution of the target program; and

executing an interrupt routine responsive to the interrupt signal.

28. (Original) The method of claim 22 further comprising:

detecting data from the hardware simulator corresponding to an interrupt signal;

in response to detecting data from the hardware simulator corresponding to an interrupt signal, applying an interrupt signal to the target processor; and

in response to the interrupt signal, allowing the target processor to execute an interrupt routine.

29. (New) A method of testing an embedded electronic systems having a target processor adapted to execute a target program, the target processor being coupled to target hardware has a physical portion and a simulated portion, the method comprising:

monitoring signals present on a plurality of externally accessible terminals of the target processor as the target processor executes the target program;

determining when the target processor is attempting to access the simulated portion of the target hardware by inputting monitored address signals into a mapping memory and outputting a stored map result from a corresponding address in the mapping memory, for each of the monitored address signals, from the mapping memory;

combining the stored map result with a target clock counter through a logical OR function;

resetting the target clock counter with an acknowledge signal from the physical portion of the target hardware.